

# Learning-Oriented Reliability Improvement of Computing Systems From Transistor to Application Level

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**Abstract**—Due to technology scaling in modern computing platforms, the safety and reliability issues have increased tremendously, which often accelerate aging, lead to permanent faults, and cause unreliable execution of applications. Failure in some computing systems like avionics may cause catastrophic consequences. Therefore, managing reliability under all circumstances of stress and environmental changes is crucial in all abstraction layers, from application to transistor levels. Machine learning techniques are recently being employed for dynamic reliability estimation and optimization. They can adapt to varying workloads and system conditions. This paper presents reliability improvement approaches from multiple perspectives—from transistor-level to application-level—and discusses their effectiveness and limitations as well as open challenges.

**Index Terms**—Aging, Cross-layer reliability, Device and circuit reliability, Dynamic reliability estimation, Error mitigation, Machine learning for systems, Task scheduling, Timing reliability.

## I. INTRODUCTION

**T**ECHNOLOGY advancement has enabled computing systems to become an integral part of human life. However, the ongoing technology scaling is introducing an ever-increasing number of reliability challenges, especially when it comes to advanced technology nodes [1], [2]. This endangers the correct operation of hardware and software of computing processors. A failure of such systems (applications or hardware) may lead to catastrophic consequences. To design a reliable system, mitigation and countermeasures against error and aging need to be applied across multiple abstraction layers of the computing system, from transistors to all the way up to the application design, since various levels may be involved in the error and aging process [3]. Several design- and run-time approaches should be exploited, which can adapt to varying system conditions, execution requirements, and workloads variations during run-time. Machine learning (ML) techniques are recently employed for dynamic reliability improvement [4]. They can effectively adapt to such variations and determine effective system configuration under dynamic and environmental changes. Although ML techniques are very promising for improving reliability, they introduce several challenges in each and across layers that need to be carefully considered.

This paper discusses various aspects of learning-based reliability monitoring and improvement in computing systems.



Fig. 1. Learning-based reliability management.

Fig. 1 shows a workflow for learning-based reliability management in which actions refer to optimization knobs used by the learning controller, states are the inputs based on the observation, and the agent aims to optimize the reward function, i.e., reliability improved in different abstraction layers, by using the resiliency models like mean time to failure (MTTF). In this paper, we first discuss how ML techniques can be used to estimate and mitigate aging from the transistor level to the standard-cell and circuit levels (Section II). Section III describes how ML can help to alleviate challenges of reliability modeling and improvement at the architectural level. Then, Section IV presents a survey of learning-based approaches that could improve reliability at the application layer through operating system (OS) techniques. We then analyze the reliability on a fault-tolerant system and discuss the timing costs in correcting register-level errors in Section V. Finally, we discuss the open challenges and limitations in Section VI and present summary in Section VII.

## II. ESTIMATING DEVICE AND CIRCUIT RELIABILITY USING CLASSICAL AND EMERGING MACHINE LEARNING

Reliability is one of colossal concerns for circuit designers. Transistor self-heating (SHE) is increasingly challenging because transistor scaling is reaching atomic levels in which quantum confinement becomes substantially prominent. With more confined 3D structures (e.g., TSMC Nanosheet FETs and Intel Ribbon FETs), heat arising in the transistor's channel cannot be easily dissipated and is hence “trapped” inside the transistor's channel. Such heat trapped inside the transistor

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